

April 16, 2004

To: Commissioner for Patents

P.O.Box 1450

Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572

28 Davis Avenue

Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/796,430 03/09/04

Chin-Shan Hou et al.

A PLACEMENT AND ROUTING METHOD TO REDUCE JOULE HEATING

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

## CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 4, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Signature/Date

TSMC-02-189/03-856

- U.S. Patent 5,811,352 to Numata et al., "Method of Making Reliable Metal Leads in High Speed LSI Semiconductors Using Dummy Leads," describes a method to reduce Joule heating in metal lines.
- U.S. Patent 5,510,293 to Numata, "Method of Making Reliable Metal Leads in High Speed LSI Semiconductors Using Thermoconductive Layers," discloses a method to reduce Joule heating in metal lines.
- U.S. Patent 5,858,869 to Chen et al., "Method for Fabricating Intermetal Dielectric Insulation Using Anisotropic Plasma Oxides and Low Dielectric Constant Polymers," teaches a method to form an intermetal dielectric layer with improved Joule heating performance.
- U.S. Patent 6,265,308 to Bronner et al., "Slotted Damascene Lines for Low Resistive Wiring Lines for Integrated Circuit," describes a method to form damascene lines and vias.

Sincerely,

Stephen B. Ackerman,

Req. No. 37761

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